

ABSTRACT

A digital signal processor performs turbo and Viterbi channel decoding in wireless systems. The computation block of the digital signal processor is provided with an accelerator for executing instructions associated with trellis computations. An ACS
5 instruction performs trellis computations of alpha and beta metrics. Multiple butterfly calculations can be performed in response to a single instruction. A TMAX instruction is used to calculate the log likelihood ratio of the trellis.

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